AMENDMENTS TO THE SPECIFICATION:

Please substitute the following amended paragraph for the pending paragraph beginning on page 6, line 17.

A time allocation section **128** determines the amount of resources determined to be available by the resource supply calculator **[126] 124** that is to be allocated to each specific project type and, within each project type, to each project based on the rules and parameters section **[120] 126**. Preferably, exceptions to the rules and parameters of section **128** or other adjustments for particular projects or specific tasks associated with a particular project can be made via I/O section **122**. Activity rules and parameters section also includes allocation rules for allocating time between factory one, factory two, and reserve time.

Please substitute the following amended paragraph for the pending paragraph beginning on page 10, line 29.

If a time imbalance does not exist at step **300**, it is determined at step **310** whether there any new projects to be added. If no new projects have been added (step **310**), the status is updated at step **320** and the process returns to step **280**. If new projects have been added at step **310** the process proceeds to **330**. The new projects are integrated and the process returns to step **250** for allocation, assignment, etc. New projects for integration include recent (ad hoc) requests for a new factory two product, nonmandatory factory one projects that have been reclassified as mandatory items, projects required for correction of newly discovered defects in a current product or project, and so forth.

Please substitute the following amended paragraph for the pending paragraph beginning on page 11, line 26.

If there is a positive time imbalance at step **3005**, it is determined in step **3006** whether the reserve time has fallen below some threshold value, e.g., due to previous time reallocations, newly integrated projects, etc. If the reserve time has fallen below some threshold value, the positive time imbalance, or some portion

thereof, is added at step **3007** to bring the reserve time up to the threshold level. The threshold level is some preselected value above which maintained reserve time is regarded as an inefficient allocation of working hours. The process then proceeds to step **3008** and it is determined if there is still a positive time imbalance. If no, the process continues to step **340**.

Please substitute the following amended paragraph for the pending paragraph beginning on page 12, line 28.

Referring now to FIG. 4, an information handling system operable to embody the present invention is shown. The hardware system **400** shown in FIG. 4 is generally representative of the hardware architecture of a computer-based information handling system of the present invention, such as data terminals **110-112**, and an information handling system embodying project planning and management system **120**. The hardware system **400** is controlled by a central processing system **402**. The central processing system **402** includes a central processing unit such as a microprocessor or microcontroller for executing programs, performing data manipulations and controlling the tasks of the hardware system **400**. Communication with the central processor **402** is implemented through a system bus **410** for transferring information among the components of the hardware system **400**. The bus **410** may include a data channel for facilitating information transfer between storage and other peripheral components of the hardware system. The bus **410** further provides the set of signals required for communication with the central processing system **402** including a data bus, address bus, and control bus. The bus **410** may comprise any state of the art bus architecture according to promulgated standards, for example industry standard architecture (ISA), extended industry standard architecture (EISA), Micro Channel Architecture (MCA), peripheral component interconnect (PCI) local bus, standards promulgated by the Institute of Electrical and Electronics Engineers (IEEE) including IEEE 488 general-purpose interface bus (GPIB), IEEE 696/S-100, and so on. Other components of the hardware system **400** include main memory **404**, and auxiliary memory **406**. The hardware system **400** may further include an auxiliary processing system **408** as required. The main memory **404** provides storage of instructions and data for

programs executing on the central processing system **402**. The main memory **404** is typically semiconductor-based memory such as dynamic random access memory (DRAM) and/or static random access memory (SRAM). Other semi-conductor-based memory types include, for example, synchronous dynamic random access memory (SDRAM), Rambus dynamic random access memory (RDRAM), ferroelectric random access memory (FRAM), and so on. The auxiliary memory **406** provides storage of instructions and data that are loaded into the main memory **404** before execution. The auxiliary memory **406** may include semiconductor based memory such as read-only memory (ROM), programmable read-only memory (PROM), erasable programmable read-only memory (EPROM), electrically erasable programmable read-only memory (EEPROM), or flash memory (block oriented memory similar to EEPROM). The auxiliary memory **406** may also include a variety of nonsemiconductor-based memories, including, but not limited to, magnetic tape, drum, floppy disk, hard disk, optical laser disk, compact disc read-only memory (CD-ROM), write once compact disc (CD-R), rewritable compact disc (CD-RW), digital versatile disc read-only memory (DVD-ROM), write once DVD (DVD-R), rewritable digital versatile disc (DVD-RAM), etc. Other varieties of memory devices are contemplated as well. The hardware system **400** may optionally include an auxiliary processing system **408** which may include one or more auxiliary processors to manage input/output, an auxiliary processor to perform floating point mathematical operations, a digital signal processor (a special-purpose microprocessor having an architecture suitable for fast execution of signal processing algorithms), a back-end processor (a slave processor subordinate to the main processing system), an additional microprocessor or controller for dual or multiple processor systems, or a coprocessor. It will be recognized that such auxiliary processors may be discrete processors or may be built in to the main processor.

Please replace the following paragraph for the pending Abstract section beginning on page 24, line 4.

A planning system for the planning and management of multiple projects includes an input (**122**) for entering project information and task information associated with each project. The project information identifies each project as being of a mandatory, nonmandatory, or ad hoc type that arises intermittently and is

subject to change. The task information describes each task to be performed by users of the system and an estimated duration of each task. Also included are a work hour calculator (**124**), an allocation engine (**128**), a schedule preparation engine (**130**), a time tracking system (**132**), and a time imbalance calculator (**134**). An allocation modification engine (**136**) reestimates the time required for completing each project based on the actual time spent and current status for each project and reallocates time to eliminate any time imbalance detected by the time imbalance calculator.

Replacement Abstract section with changes shown:

A planning system for the planning and management of multiple projects includes an input [means] (**122**) for entering project information and task information associated with each project. The project information identifies each project as being of a mandatory, nonmandatory, or ad hoc type that arises intermittently and is subject to change. The task information describes each task to be performed by users of the system and an estimated duration of each task. Also included are a [A] work hour calculator (**124**), ~~for calculating a number of working hours available for performance of the multiple projects is also provided. An~~ an allocation engine (**128**), ~~allocates a first amount of time for performance of the mandatory projects, a second amount of time for performance of the ad hoc projects, and a third amount of time to be held in reserve, wherein the sum of the first, second, and third amounts of time is less than or equal to the available hours. A~~ a schedule preparation engine (**130**), ~~prepares a schedule for performance of tasks, the schedule including an estimated time for the performance of each task. A~~ a time tracking system (**132**), ~~records actual time spent in performing the projects and the current status of each project~~ and a time imbalance calculator (**134**) ~~detects a difference between actual time spent in performance of the projects and the estimated time for performance of the projects~~. An allocation modification engine (**136**) ~~for~~ reestimates the time required for completing each project based on the actual time spent and current status for each project and reallocates time to eliminate any time imbalance detected by the time imbalance calculator.